CLAIMS

1. A field effect transistor comprising:

a SiC surface structure;

a source and a drain formed on said SiC surface structure;

an insulating structure comprising an interface control layer and an insulating layer, wherein said interface control layer includes a Group-III nitride layer having a thickness of one molecule-layer or greater and formed in contact with said SiC surface structure, and wherein said insulating layer is formed on said interface control layer from a material that is different from that of said interface control layer and that has a larger band offset with respect to a conduction layer than said interface control layer; and

a gate electrode formed on said insulating structure.

2. A field effect transistor comprising:

an SiC surface structure;

a source and a drain formed on said SiC surface structure;

an insulating structure comprising an interface control layer and an insulation layer, wherein said interface control layer is formed in contact with said SiC surface structure and it contains Al and N, said interface control layer having a thickness of one molecule-layer or greater, and wherein said insulating layer is formed on said interface control layer from a material that is different from that of said interface control layer and that has a larger band offset with respect to a conduction layer than said interface control layer; and

a gate electrode formed on said insulating structure.

3. The field effect transistor according to claim 1 or 2, wherein said interface control layer includes an AlN layer with a thickness of 6 nm or smaller.

4. The field effect transistor according to any one of claims 1 to 3, wherein said interface control layer contains at least one Group-III element of B, Al, Ga, or In, and N.

5. The field effect transistor according to claim 1 or 2, wherein said interface control layer includes a BAlN layer whose in-plane lattice constant has a mismatch of 0.5% or less with respect to the in-plane lattice constant of SiC.

6. The field effect transistor according to any one of claims 1 to 5, wherein said insulating layer includes at least one layer selected from the group consisting of a SiO_2 layer, a Si_xN_y layer, and an Al_2O_3 layer.

7. The field effect transistor according to any one of claims 1 to 5, wherein said insulating layer is either: an Al_2O_3 layer that is formed by oxidizing a deposition layer of at least one material selected from the group consisting of AlN, Al, Al_xN_y, AlAs, and AlN_xAs_{1-x}, or an Al_2O_3 layer containing small amounts of at least one of N or As.

8. The field effect transistor according to any one of claims 1 to 7, wherein said insulating layer has a multilayered film comprised of a plurality of insulating films.

9. A non-volatile memory element comprising:

an SiC surface structure;

a floating-gate structure formed on said SiC surface structure, wherein said floating-gate structure includes a first insulator barrier layer, a well layer formed of a metal or semiconductor, a second insulator barrier layer, and a gate electrode layer, wherein said first insulator barrier layer includes an interface control layer formed in contact with said SiC surface, wherein said

interface control layer contains Al and N and has a thickness of one molecule-layer or greater; and

a source and a drain layers formed on said SiC surface structure adjacent to said floating-gate structure.

10. A method for manufacturing a field effect transistor comprising the steps of:

preparing a substrate having a SiC surface structure;

forming a source and a drain on said SiC surface structure;

controlling a step structure on the surface of said SiC surface structure and cleaning said surface;

forming an interface control layer containing Al and N with a thickness of one molecule-layer or greater adjacent to said SiC surface structure, and forming an insulating structure including an insulating layer on said interface control layer from a material different from said interface control layer and having a greater band offset with respect to a conduction carrier than said interface control layer; and

forming a gate electrode on said insulating structure.